REMARKS

Claim Rejections - 35 U.S.C. §103

Claims 2 and 3 are rejected under 35 USC §103(a) as being unpatentable over Bryant et al. (U.S. Patent No. 6,100, 564) in view of Hirano (U.S. Patent No. 6, 252, 280).

In this rejection, the Examiner states, on lines 3 to 9 of item 3, that "Bryant *et al.* discloses in Figs. 4 and 5 an insulated gate type semiconductor device comprised of ... at an interface between ... directly under a gate electrode ... on the region except for said body contact region," and further interprets, on lines 9 to 11 of item 3, however, that "Bryant *et al.* do not specifically disclose a thicker insulating film at said interface than one directly under said gate electrode".

Thus, the Office acknowledges that Bryant *et al.* neither teaches nor suggests the fact that "a thickness of an insulating film provided on a surface of a first conductivity type semiconductor region positioned at the above interface is made greater than the thickness of a gate insulating film directly under a gate electrode" as defined in the current claim 2. The insulating film is shown as reference numeral 18 in Figs. 7-8. The gate is insulating film is shown as reference numeral 17 in Figs. 7-8.

However, the Office insists, on lines 12 to 14 of item 3, that "Hirano discloses an insulating film 9 with a thickness made greater than the thickness of a gate insulating film 5N with a uniform thickness directly under a gate electrode".

Eventually, the Examiner concluded, on lines 15 to 17 of item 3, that it would have been obvious to incorporate Hirano's teachings with the device of Bryant *et al.* since that would reduce

parasitic capacitance as taught by Hirano.

It is incorrect to assert that Hirano discloses film 9 with a thickness made greater than the thickness of film 5N being situated directly under a gate electrode.

Regarding Fig. 3 and Fig.4 of Hirano, it can be considered, at a glance, that the region corresponding to the body contact region of the present invention may correspond to the region which lies directly under the insulating film 9 of Hirano for example, an SOI layer 4 shown in Fig. 3 and Fig.4. It is important to understand, however, that the above region (SOI layer 4) of Hirano does not correspond to the above body contact region of the present invention. The reason is that region 4 of Hirano does not function as a region for draining carriers stored at a channel region under a gate as does the body contact region of the present invention, as explained in Page 4, lines 25 to 29 of the written description. The reason region 4 of Hirano does not function as described above is that, in Hirano, to the above region, i.e., SOI layer 4, the same voltage is applied as that of the gate electrode 6N (6P) through a W plug 21, as explained in column 5, lines 42 to 57 of the written description. In this regard, in the present invention, the body contact region must not have applied thereto the same voltage as that of the gate electrode as can be understood from reviewing Figs. 7 and 8 of the present invention. In conclusion, no region in Hirano corresponds to the body contact region of the present invention.

Further, the present invention can be characterized as well by the fact that the insulating film 18 which is thicker than the gate insulating film 17 is located on the surface of an interface area between the (first conductivity type) body contact region and the (second conductivity type) source and drain regions. This configuration is not disclosed or taught anywhere in Hirano and

Bryant *et al.*

Furthermore, in the present invention, the gate electrode is provided on the region except for the body contact region. This configuration is not disclosed or taught anywhere in Hirano.

In any event, as explained above, the element isolation insulation film 18 of Hirano does not correspond to and is very different from insulating film 18 of the present invention.

Regarding Bryan et al., in an N-type MOSFET, a separation-use gate is fabricated by a non-doped polysillicon gate so as to form a depletion layer at the polysilicon gate side, and thereby, the thickness of the gate oxide is made substantially thick to reduce the capacitance formed thereat.

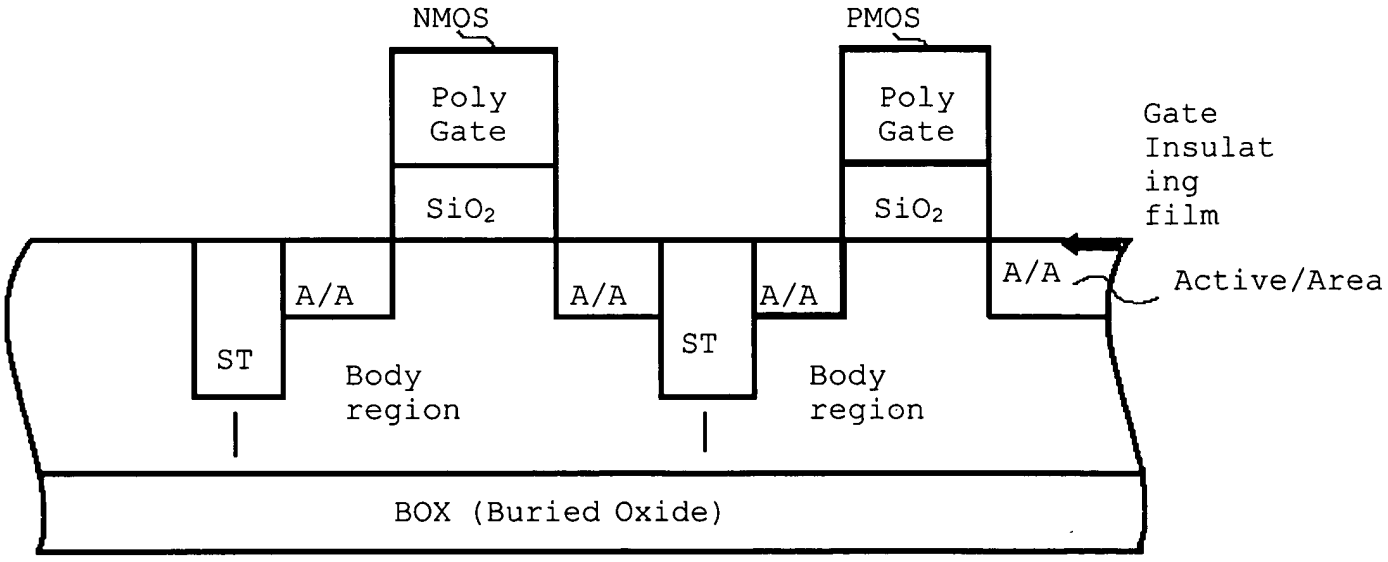
In this regard, in the present invention, such reduction of capacitance is attained by making the thickness of the insulating film (18) to be greater than that of insulating film (17) as shown in Fig. 3(c).

It should be understood that, when comparing the above two structures, the related capacitance can be reduced by making the insulating film thicker as in present invention to be more effectively than by forming the depletion layer as in Bryant *et al.*

Regarding Hirano, the semiconductor structure of Hirano is commonly called a DTMOS structure, in which the body potential is dynamically varied, usually the body potential is the same as the gate voltage, i.e., the threshold voltage V_{TH} is lowered to increase the drive capability when the device is in an usual operation mode. On the other hand, the above threshold voltage V_{TH} is recovered to reduce a leakage current when the above device is in a standby mode. In the device, the region under the gate electrode can be called a body region and it becomes necessary to employ a body contact region in order to control the potential is usually supplied with V_{DD} or V_{SS}, and the

body contact region is commonly called a "well contact".

A difference between Hirano and the present invention resides in the location of the above separation-use gate electrode. To be specific, the separation-use gate electrode is formed, in the present invention, on an active region, while the separation-use gate electrode is formed, in Hirano, on the field of the semiconductor device. In other words, the oxide film of Hirano is LOCOS or Shallow Trench Isolation (STI) for isolating a PMOS and an NMOS. Therefore, the above oxide film is very different from the gate insulating film of the present invention. Thus, the present invention requires a special separation-use polysilicon gate for separating the transistor region from the body contact region, while, in Hirano, such a special separation-use polysilicon gate is not needed but a conventional separation structure (STI) is used as illustrated below.



In view of the above discussions, current claims 2 and 3 are accordingly amended.

Specifically, in claim 2, first, the phrase "an insulating film" (18) is replaced by a first

insulating film and the phrase "a gate insulating film" (17) is replaced by a second insulating film, acting as a gate insulating film. These changes are implemented so as to better distinguish each of the two major insulating films. Further, the function of the body contact region is recited in claim 2 so as to further differentiate the current claim 2 from Hirano.

Further, current claim 3 is converted from an independent claim to a dependent claim, which depends on the newly amended claim 2. The amended claim 3 defines the "first insulating layer" of claim 2 to be "buried insulating film" (50).

Reconsideration and withdrawal of this rejection are respectfully requested.

Allowable Subject Matter

The allowance of claims 1, 5 and 9 is noted with appreciation.

Prior Art Indicated To Be Pertinent To The Disclosure

The Office has provided a list of prior art indicated to be pertinent to the Applicant's invention. Consistent with the understanding as stipulated in MPEP 706.02 that only the best prior art should be applied, this list of prior art not having been applied by the Office, it is the Applicant's understanding that the Office must have considered the listed prior art to be no more pertinent than the applied prior art of record.

CONCLUSION

In view of the aforementioned amendments and accompanying remarks, all pending claims are believed to be in condition for allowance, which action, at an early date, is requested.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 50-2866.

Respectfully Submitted,

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